Amendments to the CLAIMS:

Without prejudice, this listing of the claims replaces all prior versions and listings of the claims in the present application:

LISTING OF CLAIMS:

1. (Currently Amended) A data selection apparatus comprising:

search units each of which search units includes table search circuits and a first circuit which performs a first selection process in which a table search circuit which outputs data is selected from table search circuits each of which succeeds in a search based on input data; and

a second circuit which performs a second selection process in which a search unit which outputs data is selected from search units each of which includes a table search circuit which succeeds in a search;

wherein:

when said first circuit receives a first signal which indicates that there is a table search circuit which succeeds in a search, said first circuit sends a second signal to said second circuit before performing said first selection process, said second signal indicating that there is at least one table search circuit which succeeds in a search;

said second circuit performs said second selection process when said second circuit receives said second signal; [[and]]

a search unit which is selected by said second selection process outputs data of a table search circuit that is selected by said first selection process; and

said first selection process and said second selection process are performed in parallel at least in part so that output data of a table search circuit is selected.

2. (Original) The data selection apparatus as claimed in claim 1, wherein each of said search units has a third circuit, outside of said first circuit, which third circuit sends said first signal to said second circuit; and

said first circuit performs said first selection process at the same time as when said third circuit sends said first signal to said second circuit.

3. (Original) The data selection apparatus as claimed in claim 1, wherein each of said table search circuits is a CAM.

4. (Original) The data selection apparatus as claimed in claim 1, wherein each of said table search circuits includes a RAM and an MPU.

5. (Original) The data selection apparatus as claimed in claim 3, wherein said first circuit includes a CAM output control circuit including small-scale logic circuits divided by flip-flops in which time series pipeline processing is performed; and

said second circuit also includes small-scale logic circuits divided by flip-flops in which time series pipeline processing is performed.

6. (Canceled).

7. (Currently Amended) ~~The data selection apparatus as claimed in claim 6, further comprising:~~ A data selection apparatus comprising:

search units each of which search units comprises table search circuits and a data output control circuit, said table search circuit selecting data from a stored data table, which data includes an entry matching a search key which is a bit sequence of a part of input data, said data output control circuit performing a first selection process in which the highest priority output data is selected from outputs of said table search circuits;

a unit output control device which performs a second selection process in which the highest priority output data is selected from outputs of said search units;

data search success signal output means which sends a data search success signal to said data output control circuit from a hit circuit which is a table search circuit which succeeds in a search;

unit search success signal output means which sends a unit search success signal indicating that there is at least said hit circuit in said search unit to said unit output control device before said data output control device performs said first selection process,

wherein said data output control device starts said first selection process upon receiving said data search success signal and said unit output control device starts said second selection

process upon receiving said unit search success signal, and a data output control circuit in a search unit which is selected by said unit output control device selects output data of a table search circuit[[,]];

first stage search units each of which is said search unit;

nth (n 2) stage search units each of which nth stage search units includes (n-1)th stage search units and an (n-1)th stage unit output control device which selects the highest priority (n-1)th stage search unit from said (n-1)th stage search units; and

an nth stage unit output control device which selects the highest priority nth stage search unit from said nth stage search units;

wherein said (n-1)th stage unit output control devices send nth stage unit search success signals to said nth stage unit output control device before each of said (n-1)th stage unit output control device selects an (n-1)th stage search unit; and

wherein an (n-1)th stage search unit output selection process in said (n-1)th stage unit output control devices and an nth stage search unit output selection process in said nth stage unit output control device are performed in parallel at least in part so that output data of a table search circuit is selected.

8. (Original) The data selection apparatus as claimed in claim 7, wherein each of said first stage search units sends a unit search success signal to unit output control devices of second or later stages instead of (k-1)th (2 k n) stage unit output control devices sending said unit search success signal to a kth stage unit output control device.

9. (Currently Amended) The data selection apparatus as claimed in claim [[6]] 7, wherein said data output control circuit includes a CAM output control circuit including small-scale logic circuits divided by flip-flops in which time series pipeline processing is performed[[;]], and said unit output control device also includes small-scale logic circuits divided by flip-flops in which time series pipeline processing is performed.

10. (Currently Amended) The data selection apparatus as claimed in claim 7, wherein said data output control circuit includes a CAM output control circuit including small-scale logic circuits divided by flip-flops in which time series pipeline processing is performed[[;]], and

said unit output control device also includes small-scale logic circuits divided by flip-flops in which time series pipeline processing is performed

11. (Currently Amended) The data selection apparatus as claimed in claim [[6]] 7, wherein each of said table search circuits includes a RAM and an MPU.

12. (Original) The data selection apparatus as claimed in claim 7, wherein each of said table search circuits includes a RAM and an MPU.

13. (Currently Amended) A packet processing apparatus including a data selection apparatus, said data selection apparatus comprising:

search units each of which search units includes table search circuits and a first circuit which performs a first selection process in which a table search circuit which outputs data is selected from table search circuits each of which succeeds in a search based on an input packet; and

a second circuit which performs a second selection process in which a search unit which outputs data is selected from search units each of which includes a table search circuit which succeeds in a search;

wherein:

when said first circuit receives a first signal which indicates that there is a table search circuit which succeeds in a search, said first circuit sends a second signal to said second circuit before performing said first selection process, said second signal indicating that there is at least one table search circuit which succeeds in a search;

said second circuit performs said second selection process when said second circuit receives said second signal; [[and]]

a search unit which is selected by said second selection process outputs data of a table search circuit that is selected by said first selection process, said data being used as a destination address to which said input packet is transferred; and

said first selection process and said second selection process are performed in parallel at least in part so that output data of a table search circuit is selected.

14. (Original)The packet processing apparatus as claimed in claim 13, wherein each of said search units has a third circuit, outside of said first circuit, which third circuit sends said first signal to said second circuit; and

said first circuit performs said first selection process at the same time as when said third circuit sends said first signal to said second circuit.

15. (Canceled).

16. (Currently Amended) ~~The packet processing apparatus as claimed in claim 15, said data selection apparatus further comprising:~~ A packet processing apparatus including a data selection apparatus, said data selection apparatus comprising:

search units each of which search units comprises table search circuits and a data output control circuit, said table search circuit selecting data from a stored data table, which data includes an entry matching a search key which is a bit sequence of a part of an input packet, said data output control circuit performing a first selection process in which the highest priority output data is selected from outputs of said table search circuits;

a unit output control device which performs a second selection process in which the highest priority output data is selected from outputs of said search units;

data search success signal output means which sends a data search success signal to said data output control circuit from a hit circuit which is a table search circuit which succeeds in a search; and

unit search success signal output means which sends a unit search success signal indicating that there is at least said hit circuit in said search unit to said unit output control device before said data output control device performs said first selection process,

wherein said data output control device starts said first selection process upon receiving said data search success signal and said unit output control device starts said second selection process upon receiving said unit search success signal, and a data output control circuit in a search unit which is selected by said unit output control device selects output data of a table search circuit, said output data being used as a destination address to which said input packet is transferred;[[,]]

first stage search units each of which is said search unit;

nth (n 2) stage search units each of which nth stage search units includes (n-1)th stage search units and an (n-1)th stage unit output control device which selects the highest priority (n-1)th stage search unit from said (n-1)th stage search units; and

an nth stage unit output control device which selects the highest priority nth stage search unit from said nth stage search units;

wherein said (n-1)th stage unit output control devices send nth stage unit search success signals to said nth stage unit output control device before each of said (n-1)th stage unit output control device selects an (n-1)th stage search unit; and

wherein an (n-1)th stage search unit output selection process in said (n-1)th stage unit output control devices and an nth stage search unit output selection process in said nth stage unit output control device are performed in parallel at least in part so that output data of a table search circuit is selected.

17. (Original) The packet processing apparatus as claimed in claim 16, wherein each of said first stage search units sends a unit search success signal to unit output control devices of second or later stages instead of (k-1)th (2 k n) stage unit output control devices sending said unit search success signal to a kth stage unit output control device.